No. 09/596,103 filed June 16, 2000, U.S. Patent Application Serial No. 09/598,567 filed June 21, 2000, U.S. Patent Application Serial No. 09/598,564 filed June 21, 2000, U.S. Patent Application Serial No. 09/598,566 filed June 21, 2000, U.S. Patent Application Serial No. 09/598,558 filed June 21, 2000, U.S. Patent Application Serial No. 09/598,084 filed June 21, 2000, U.S. Patent Application Serial No. 09/599,980 filed June 22, 2000, U.S. Patent Application Serial No. 09/711,218 filed November 9, 2000, U.S. Patent Application Serial No. 09/747,056 filed December 12, 2000, U.S. Patent Application Serial No. 09/853,989 filed May 11, 2001, U.S. Patent Application Serial No. 09/886,855 filed June 21, 2001, U.S. Patent Application Serial No. 09/791,940 filed February 23, 2001, U.S. Patent Application Serial No. 09/792,819 filed February 23, 2001, U.S. Patent Application Serial No. 09/792,256 filed February 23, 2001, U.S. Patent Application Serial No. 10/013,908 entitled "Methods and Apparatus for Efficient Vocoder Implementations" filed October 19, 2001, Provisional Application Serial No. 60/251,072 filed December 4, 2000, Provisional Application Serial No. 60/281,523 filed April 4, 2001, Provisional Application Serial No. 60/283,582 filed April 13, 2001, Provisional Application Serial No. 60/287,270 filed April 27, 2001, Provisional Application Serial No. 60/288,965 filed May 4, 2001, Provisional Application Serial No. 60/298,624 filed June 15, 2001, Provisional Application Serial No. 60/298,695 filed June 15, 2001, Provisional Application Serial No. 60/298,696 filed June 15, 2001, Provisional Application Serial No. 60/318,745 filed September 11, 2001, Provisional Application Serial No. 60/340,680 entitled "Methods and Apparatus for Video Coding" filed October 30, 2001, Provisional Application Serial No. 60/335,157 entitled "Methods and Apparatus for a Bit Rate Instruction" filed November 1, 2001, all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.

In a presently preferred embodiment of the present invention, a ManArray 2x2 iVLIW single instruction multiple data stream (SIMD) processor 100 shown in Fig. 1 contains a controller sequence processor (SP) combined with processing element-0 (PE0) SP/PE0 101, as described in further detail in U.S. Application Serial No. 09/169,072 entitled "Methods and Apparatus for Dynamically Merging an Array Controller with an Array Processing Element". Three additional PEs 151, 153, and 155 are also utilized. It is noted that the PEs can be also labeled with their matrix positions as shown in parentheses for PE0 (PE00) 101, PE1 (PE01)151, PE2 (PE10) 153, and PE3 (PE11) 155.

The SP/PE0 101 contains a fetch controller 103 to allow the fetching of short instruction words (SIWs) from a 32-bit instruction memory 105. The fetch controller 103 provides the typical functions needed in a programmable processor such as a program counter